Standard Cell Characterization

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Overview

- Basics
- Reasons for Characterization
- Characterization Flow
- Characterization Parameters
- Models
- Measurement & Verification
- Library Formats
- Summary
- Sources & Acknowledgments
Basics

• **Standard Cells**
  
  – Logic units of similar geometry (same height)
  
  – Implement basic logic (NAND, NOR, INV, FF, LATCH, complex gates, …)
  
  – Usually come in libraries for a specific technology

Prof. P. Fischer: “Digitale Schaltungstechnik”
Basics

• **Use (Flow)**
  - Hardware is described in higher level language (e.g. RTL)
  - Description is translated in Boolean logic and sequential elements
  - The logic is mapped on standard cells
  - Standard cells are placed in rows
  - Cells are properly connected by routing channels and/or additional metal layers

Prof. P. Fischer: “Digitale Schaltungstechnik”
Reasons for Characterization

• **Problems of Standard Cells in polygon level format (GDSII)**
  – Extraction of functionality is complicated and unnecessary as it is known
  – Functional/Delay simulation takes way too long
  – Power extraction for a whole chip takes too long
  – Automatic detection of timing constraints (e.g. Setup time) is difficult

• **Solution**
  – A simple model for delay, function, constraints and power on cell/gate level => cell characterization
Characterization Flow

- **Netlist Extraction**
  - Transistors, resistances and capacitances are extracted with special tools and saved as SPICE netlist (or similar)

- **Specification of parameters**
  - Library-wide parameters have to be specified: e.g. max Transition time, PVT-corners

- **Model selection and specification**
  - The used models determine the required data
Characterization Flow

- **Measurement**
  - The cells are simulated with a SPICE-like tool to obtain the required data

- **Model Generation**
  - The obtained data is fed into the models
  - Completes characterization itself

- **Verification**
  - Different checks are performed to ensure the correctness of the characterization
Characterization Flow

Knowledge Database
I-Slew, O-Load
PVTs, NxN
LPE Flow

Extraction

SPICE netlist

PVT Characterization

Timing, Power, Database

Model Generation

EDA Vendor (Model)

Synopsys (.LIB)

Cadence (TLF)

GDS2

Knowledge Database

Power, SI, etc.

Synopsys timing

Cadence timing

Model Verification

Model Verification

Model Verification

Trend Checks

"Model Generation & Verification"; Artisan Presentation Page 40
Characterization Parameters

- **Global Parameters**
  - PVT Corner Selection (Process, Voltage, Temperature)
  - Unit Definition (e.g. Standard Load)
  - Default Definition
  - Threshold values (Transition Thresholds, ...)
  - Limits (max. Output Load, max. Transition time, ...)
  - Wireload Models

Transition Time: Characterized and Measured

Transition Time: Standardized Reporting

"Transition Time": Artisan Presentation Page 23
Characterization Parameters

- **For mapping, functional simulation**
  - Functionality

- **For optimization, delay simulation**
  - Area
  - Power
  - Timing constraints (Setup/Hold time, Recovery/Removal time)
  - Propagation Delay time
  - Requires:
    - Input Capacitance
    - Transition time
      (Output Slew)

"Setup and Hold Constraints"; Library Compiler User Guide; Fig 3-10
Characterization Parameters

- **For Power extraction, IR-Drop analysis, EM analysis**
  - Dynamic Power (switching power)
  - Static Power (leakage power)
  - Passive power (internal power)
    (power used by sequential cells (e.g. flip-flops) when inputs (clock too) change without output change)
  - Same Requirements as Delay

- **For Place & Route**
  - Geometry (cell width)
  - Pin locations
  - Routing channels (metal areas not used by a cell) and Routing obstructions (additional metal areas used by cell)
Models

• **Simple Models**
  – Functionality, geometry, capacitance

• **Propagation Delay and Transition Time**
  – Both are usually modeled together in the same way

• **Power**
  – Depends on the same values as the Propagation Delay
    => often modeled analogical to Propagation Delay

• **Constraints**
  – Usually as fixed timing values
Delay Models

- **Generic CMOS Delay Model:**
  - Sum of Intrinsic delay, Slope delay, Transition delay and Connect delay
  - Intrinsic delay is a fixed value which models delays independent of the surroundings
  - Slope delay is produced by the slew of the input signal. The input slew is multiplied with a sensitivity factor
  - Transition delay is the time required to charge the capacitance of the next stage input pins
  - Connect Delay is delay produced by the RC value of the wire to the next stage input pin and the capacitance of the next stage input pins
Delay Models

- **CMOS Non-linear Delay Model:**
  - Very common
  - Delay and Transition time are modeled as functions of Input slew and Output load
  - The data is stored as a 2-dimensional lookup-table
  - Intermediate values are interpolated
  - Data point are usually not equidistant

“Result of Delay Calculation”
Synopsys; Library Compiler User Guide, Figure 2-7
Delay Models

- **Scalable Polynomial Delay Model:**
  - Data is stored as polynomial approximation
  - PVT-Parameters are input values themselves
    => only one characterization file necessary
  - The Polynomial may depend on Input slew, Output load, Voltage, Temperature and a Second voltage for level shifter cells
  - The Polynomial can be piecewise defined

- **CMOS Piecewise Linear Delay Model:**
  - Like the generic model
  - Uses piece linear (constant) functions instead of proportional functions
Delay Models

• **Delay Calculation Module (DCM):**
  – Delay information is stored in a special DCM file
  – Does not store parameters of an equation but a sort of programming code (Delay Calculation Language (DCL))
  – Very flexible since not bound to a specific model
  – Defined in IEEE 1481.1
  – Also called DPCM (delay and power calculation module)
Power Models

• **Static Power Model**
  – Each cell is assigned a fixed power consumption

• **Complex Power Model**
  – Leakage power
    • Fix value: average or per state
  – Internal/Passive power
    • 1D-lookup table depending on input slew
  – Switching/Dynamic power
    • Simple: const * output load
    • Complex: 2D-lookup table: depending on Input Slew and Output Load
      sometimes even per state
Measurement & Verification

- **Simulation**
  - Extracted netlist is simulated with a SPICE-like tool
  - Every required data point is processed (pass mill method)
  - Temperature sweeps and simulations with varying element parameters (Monte Carlo simulation) give information about result reliability
  - Constraints are found by binary search

- **Physical**
  - Creation of chip with all cells and special testing logic (see next page)
  - Measurement of cells with probing tool
  - E.g. INV-chain is used to measure typical delay

“Combinational Cell Test Circuits”; Artisan Presentation Page 48
Measurement & Verification

Control Block
- Gray Counter
- Binary Counter

Functional Block
- Mux
- All Core Cells
- Mux Tree

Timing Block
- Delay Chains
- Setup Hold block
- Mux Tree

"Standard Cell – Block Diagram"; Artisan Presentation Page 47
Measurement & Verification

• Trend Checks
  – Checks if values like capacitances are in expected range
  – Checks if models behave like expected
    • Higher load => higher delay
    • Higher input slew => higher transition time
    • Higher driving strength => lower delay
    • Higher temperature => higher delay
    • ...

• Test Designs
  – Typical design is created with standard tools
  – Checked for functionality and technology rule violations
Library Formats

• **Synopsys Liberty Library (LIB)**
  – Used by Synopsys products
  – Synthesis, Timing and Power
  – Supports most models
  – Virtually a standard
  – Can be compiled (.db)

• **Timing Library Format (TLF)**
  – Used by Cadence products
  – Synthesis, Timing and Power
  – Same features as .lib
  – Can be compiled
Library Formats

• **Delay and Power Calculation System (DPCS)**
  – Defined by IEEE 1481.1
  – Timing and Power. No Synthesis
  – Uses the Delay and Power Calculation Module (DCM/DPCM) instead of discrete values

• **Open Library API (OLA)**
  – Open-source extension to IEEE 1481.1 (DPCS)
  – Includes functional information for synthesis
Library Formats

- **Advanced Library Format (ALF)**
  - Extension to the .lib - Format
  - Binary

- **Library Exchange Format (LEF)**
  - Place & Route

- **Synopsys Stamp Model**
  - Used to describe large blocks (e.g. RAM)

- **Verilog/VHDL**
  - For simulation only
Summary

- Characterization is necessary for the use of Standard Cells
- Characterization is done on extracted netlists
- The Non-linear Delay Model is the most common one
- The Synopsys Liberty Format (.lib) is virtually standard with the Cadence Timing Library Format (.tlf) as number two
- Smaller feature sizes require more accurate models
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Sources

• **Artisan Components, Inc.**
  – Presentation: “Artisan Standard Cell Products Overview”

• **Cadence**
  – Aptivia User Guide

• **Synopsys**
  – Library Compiler User Guide

• **Prof. Dr. P. Fischer**
  – Script: “Digitale Schaltungstechnik”